

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277
Craig HANSEN, et al. : Confirmation Number: To be assigned
Serial No.: Unknown : Group Art Unit: To be assigned

Continuation of :
Application No. 10/646,787 :
Filed August 25, 2003 :
Filed: January 16, 2004 : Examiner: To be assigned

For: **MULTITHREADED PROGRAMMABLE PROCESSOR AND SYSTEM WITH PARTITIONED OPERATIONS**

INFORMATION DISCLOSURE STATEMENT

Mail Stop NEW APPLICATIONS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

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Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY


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Date: January 16, 2004

WDC99 845008-1.043876.0153

INFORMATION DISCLOSURE CITATION IN AN APPLICATION		ATTY. DOCKET NO. 43876-153	SERIAL NO. Continuation of Serial No. 10/646,787
		APPLICANT HANSEN, et al.	
(PTO-1449)		FILING DATE January 16, 2004	GROUP To be assigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,025,772	05/24/77	Constant			
	4,489,393	12/18/84	Kawahara, et al.			
	4,701,875	10/20/87	Konishi, et al.			
	4,727,505	02/23/88	Konishi, et al.			
	4,876,660	10/24/89	Owens, et al.			
	4,893,267	01/09/90	Alsup, et al.			
	4,956,801	09/11/90	Priem et al.			
	4,969,118	11/06/90	Montoye, et al.			
	4,975,868	12/04/90	Freerksen			
	5,032,865	07/16/91	Schlunt			
	5,157,388	10/20/92	Kohn			
	5,201,056	04/06/93	Daniel, et al.			
	5,268,855	12/07/93	Mason, et al.			
	5,268,995	12/07/93	Diefendorff, et al.			

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EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation
						Yes No

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	Parallel Computers for Graphics Applications, Adam Levinthal, Pat Hanrahan, Mike Paquette, Jim Lawson, Pixar San Rafael, California, 1987
	Organization of the Motorola 88110 Superscalar RISC Microprocessor, Keith Diefendorff and Michael Allen.
	Microprocessor Report, Volume 7 Number 13, October 4, 1993, IBM Regains Performance Lead with Power2, Six Way Superscalar CPU in MCM Achieves 126 SPECint92.
	IBM Creates PowerPC Processors for AS/400, Two New CPU's Implement 64-Bit Power PC with Extensions by Linley Gwennap, July 31, 1995.

EXAMINER	DATE CONSIDERED
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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,408,581	04/18/95	Suzuki, et al.			
	5,423,051	06/06/95	Fuller, et al.			
	5,426,600	06/20/95	Nakagawa, et al.			
	5,500,811	03/19/96	Corry			
	5,557,724	09/17/96	Sampat, et al.			
	5,588,152	12/24/96	Dapp, et al.			
	5,592,405	01/07/97	Gove, et al.			
	5,640,543	06/17/97	Farrell, et al.			
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	5,666,298	09/09/97	Peleg, et al.			
	5,669,010	09/16/97	Duluk, Jr.			
	5,673,407	09/30/97	Poland, et al.			
	5,675,526	10/07/97	Peleg, et al.			
	5,680,338	10/21/97	Agarwal, et al.			

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EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
	0 474 246 A2	06/09/91	Europe				
	0 654 733 A1	05/07/94	Europe				

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	The Visual Instruction Set (VIS) in UltraSPAR TM , L. Kohn, G. Maturana, M. Tremblay, A. Prabhu, G. Zyner, May 3, 1995, 462-469
	Osborne McGraw-Hill, i860 TM Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn, 1990, 8-10, 171-175, 182-183
	A General-Purpose Array Processor for Seismic Processing, Nov-Dec., 1984, Volume 1, No. 3) Revisiting past digital signal processor technology, Don Shaver- Jan-Mar. 1998, 15th Anniversary Issue, 5-26
	Accelerating Multimedia with Enhanced Microprocessors, Ruby B. Lee, IEEE Micro., April 1995, 22-32
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EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,721,892	02/24/98	Peleg, et al.			
	5,734,874	03/31/98	Van Hook, et al.			
	5,757,432	05/26/98	Dulong, et al.			
	5,758,176	05/26/98	Agarwal, et al.			
	5,802,336	09/01/98	Peleg, et al.			
	5,809,292	09/15/98	Wilkinson, et al.			
	5,818,739	10/06/98	Peleg, et al.			
	5,825,677	10/20/98	Agarwal, et al.			
	5,835,782	11/10/98	Chu Lin, et al.			
	5,886,732	03/23/99	Humbleman			
	5,922,066	07/13/99	Cho, et al.			
	5,983,257	11/09/99	Dulong, et al.			
	6,016,538	01/18/00	Guttag, et al.			
	6,092,094	07/18/00	Ireton			
	6,401,194 B1	06/04/02	Nguyen, et al.			
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WDC99 864084-1.043876.0153

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

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EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ₂ (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US	4,785,393	11/15/1988	Chu et al.	
	US	4,814,976	03/21/1989	Craig C. Hansen, et al.	
	US	5,031,135	07/09/1991	Patel	
	US	5,280,598	01/1994	Osaki et al.	
	US	5,481,686	01/02/1996	Dockser	
	US	5,487,024	01/1996	Girardeau Jr.	
	US	5,600,814	02/1997	Gahan et al.	
	US	5,740,093	04/14/1998	Sharangpani	
	US	5,742,840	04/21/1998	Hansen et al.	
	US	5,768,546	06/1998	Kwon	
	US	5,898,849	04/27/1999	Tran	
	US	5,996,057	11/30/1999	Hunter L. Scales, III, et al.	
	US	6,041,404	03/21/2000	Patrice Roussel, et al.	
	US	6,052,769	04/18/2000	Thomas R. Huff, et al	
	US	6,173,393 B1	01/09/2001	Salvador Palanca, et al.	
	US	6,275,834 B1	08/14/2001	Derrick Chu Lin, et al	
	US	6,295,599	09/2001	Hansen et al.	

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						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications And Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (March 1992)
		IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995)
		IBM, "The PowerPC Architecture: A Specification For A New Family of Risc Processors", 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994).
		Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set", Manual Part No. 09740-90039, (1990).
		MIPS Computer Systems, Inc., "MIPS R4000 User's Manual", Mfg. Part No. M8-00040, (1990).

EXAMINER

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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	US	5,819,101	10/6/1998	Alexander Peleg, et al			
	US	5,881,275	3/9/1999	Alexander Peleg, et al			
	US	6,119,216	9/12/2000	Alexander Peleg, et al			
	US	6,516,406	2/4/2003	Alexander Peleg, et al			
	US	6,539,467	3/25/2003	Timothy D. Anderson, et al			
	US	6,574,724	6/3/2003	David Hoyle, et al			
	US	6,631,389 B2	10/7/2003	Derrick Chu Lin, et al			
	US						
	US						
	US						
	US						
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